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Performance Evaluation of Carry Select Adder-Review

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Abstract

Arithmetic circuit is the fundamental block of many processor architectures such as digital signal processors and advanced microprocessor design. Adders form an almost mandatory component of every contemporary integrated circuit. Carry Select Adder (CSLA) used to achieve the fast addition operation, this is the high speed adders used in many DSP operations to perform accumulation operation. Speed is to be considered as an indispensable parameter, before that power dissipation is one of the most important design goals in many ICs. In digital adders, the speed of addition is limited by the time required to propagate a carry through the adder. Several approaches have been proposed for the solution of this problem but development is currently still very much in progress. To overcome this problem Binary to Excess-1 Convertor (BEC), Sharing the Common Boolean Logic term and Gate-level modifications are used to improve the ADP parameters. The carry-select method is considered to be a good compromise between cost and performance in carry propagation adder design. Carry select adder is being able to calculate all the input bits nearly simultaneously. This article primarily deals the 4-,8-,16-,32-,64-Bit CSLA adders and various methods which is involved to reduce the Area, Delay, Power under several criteria.

Keywords: Arithmetic units, CSLA, BEC, Low power, High speed, Reduced area.

Introduction

Many digital systems use the basic operation such as addition and subtraction. Addition is a strong operation than the multiplication and subtraction. So addition places a vital role than the subtraction to perform many addition functions in Arithmetic logic unit, High speed multiplication, FIR filters, Various computational systems etc. Some other applications of adders are in Multiply – Accumulate (MAC) structures. Adders are also used in multipliers, in high speed integrated circuits and many digital signal processing to execute various algorithms such as IIR, FIR and FFT. Digital adder performs the operation of accumulation; these are the most widely used components in such circuits. Even though this may also create some delay during process; so that reduction in speed may also happen. Minimizing area and power is the more challenging task in modern VLSI design. To design a low power and area efficient adder circuit this is the greatest important area of today's VLSI research.

Carry-Select Adder is a specific way to implement the adder, and it has a logic element that computes the (n+1)-bit sum of two n-bit numbers. The adder design is simple but pretty faster, then having a gate level depth of $0(\sqrt{n})$. This generally consists of two Ripple Carry Adder (RCA) and a multiplexer. RCA has least intricate circuit but this adder is not worthy for practical use because the speed of addition in RCA is restricted by the carry signal that ripples through the adder. Adding two n-bit numbers to a carry-select adder is done with two adders (hence two ripple carry adders) in order to perform the calculation twice during operation, one time with the assumption of the carry being zero and the other assuming one. After the two consequences are calculated, an exact sum as well as the exact carry, is then selected with the multiplexer once the accurate carry is known.

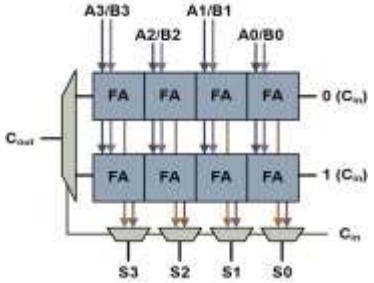

Fig.1 4-Bit CSLA

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In RCA, the sum for each bit position entails a carry from prior stage. CSLA relieves the problem occurred in carry propagation delay and therefore performs of the addition operation becomes more faster. However, the CSLA is not area efficient because it uses multiple pairs of RCA to generate partial sum and carry by allowing carry input and then the final sum and carry are carefully chosen by the multiplexers (mux).

The adder system is defined to increases the speed of the addition process by reducing the carry-propagation time to the minimum corresponding with economical circuit design. The demanding in carry-propagation delay is overcome by independently generating multiple-radix carries and using these carries to select between at the same generated sums. These articles discuss the 4-bit, 8-bit 16-bit adders and various methods which are involved to reduce the ADP under several criteria in Digital Signal Processing.

Various methods to analyze the performance of CSLA

4-Bit CSLA

[1] Shuchi Verma.V 2014 Initially the regular CSLA structure is altered by using BEC unit. Then modified CSLA is designed with the help of D-latch and without using mux the adder is designed. It deals with the design & analysis of Carry Select Adder. In this the proposed adders are designed by using 0.18µm CMOS process technology & simulated with Modelsim 6.3f. For N bit RCA the delay is linearly proportional to N bit. These implement the BEC approach to reduce the delay and area of the adder. By cascading the RCA CSLA is designed. One RCA carries the Cin=0 and other carries with Cin=1. Based on this technique 16-bit CSLA is designed. The gate count is determined by using the number of half adder, full adder and mux. Gate Count=HA+FA+MUX.

[2] Bhuvaneshwaran et all-2013 minimizing area and power is the more challenging task in modern VLSI design. The design of area and power effective high-speed data path logic systems forms the major areas of research in VLSI system design. This grants a new dynamic logic entitled sp-D3L that overcomes the high speed limitations of D3L. Power intake is significantly reduced by using the sp-D3L logic. CSLA is one of the fastest adders used in many data-processing processors to perform fast arithmetic functions. From the whole design system of CSLA, it is clear that there is duration for reducing the area and power consumption in the CSLA.

[3] Swarnalatha.K et all-2013 work uses a simple and efficient gate-level modification to significantly reduce the area and power of the CSLA. A Carry Select Adder is one of the key hardware blocks in most digital and high performance systems. The design of CSLA which offer either high speed, low power consumption, regularity of layout less area and compressed VLSI implementation. Researchers suggest that Ripple Carry Adder had a lesser area while having minor speed, in contrast to which Carry Select Adders are having high speed but retain a larger area.

[4] Rama Krishna Reddy.J et all-2013 the regular SQRT CSLA involve the two RCA units along with carry input as 1 and 0. Then the final sum will be designated from multiplexers (Mux) via the carry out generated by the penetrable block. An efficient carry select adder with logical reduction of excess redundant hardware is designed by using this method with the reduction of ADP. The performance of the adder is evaluated by using 90-ηm CMOS Technology in Cadence Tools. For 16-bit regular SQRT CSLA there is a reduction of basic logic gates from 434 to 323.The delay is reduced by interchanging the Full-adder with a half-adder in principal bit of every RCA. This will reduces the number of iterations required to get the final sum. Final architecture is implemented using the RCA with carry input as 1, along with a single multiplexer, Or gate and And gate.

[5] Hemima, R. et all-2011 from the structure of the CSLA, it is clear that there is a possibility for dropping the area and power intake in the CSLA. This effort uses a simple and efficient transistor level modification to significantly reduce the area and power of the CSLA. Based on this modification 4-bit CSLA architecture have been developed and compared with the regular CSLA architecture. That design will reduce the area and power as compared with the fixed CSLA with only minor increase in the delay. It estimate estimates the performance of the new CSLA designs in terms of delay, area, power, and their products with logical effort and finished custom design adn drawn with the help of 0.18-µm CMOS process technology.

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Table-1. Comparison of ADP

Adder	*Area (mm)*	*Delay (ns)*	*Power (mW)*
1.CSLA	32	-	9.519
2.CSLA	6	-	36.43
3.CSLA	105	8	-
4.CSLA	51	0.294	4.420
5.CSLA	-	4.653	62.4

8-bit CSLA:

[6] Damarla Paradhasaradhi-2013 describes the design of Integrated Circuits; area tenancy plays an essential role because of growing the inevitability of portable systems. A new method of area-efficient carry select adder by sharing the Common Boolean logic term (CBL) is proposed. Next step of logic simplification and sharing partial circuit, only unique XOR gate and inverter gate in each summation operation as well as one AND gate and one inverter gate in each carry-out operation are needed. Over the multiplexer, the correct output is selected according to the logic states of the carry in signal. An area-efficient carry select adder by sharing the CBL term is used to remove the duplicated adder cells in the conventional carry select adder. Based on this modification a new architecture has been developed. The modified CSLA architecture has been established using Binary to Excess-1 converter (BEC). The 8-bit inputs are directly given to the full adder to complete the 8-bit sum and carry. The proposed architecture will reduced area and delay as compared with the regular SQRT CSLA architecture.

[7] Pallavi Saxena-2013 proposed the Binary to Excess- 1 converter (BEC) method and Common Boolean Logic term. Integrated circuit technology, adder is a digital circuit which performs addition of numbers. The structure of CSLA is such that there is further scope of decreasing the area, delay and power consumption. Simple and efficient gate – level modification is used in order to reduce the ADP of CSLA. The conventional carry select adder has the disadvantage of more power consumption and occupying more chip area. To avoid such a problem in CSLA, this uses the BEC method instead of RCA with Cin=1 in conventional CSLA in order to reduce the area and power. Because BEC uses less number of logic gates than N-bit full adder structure. To replace the N-bit RCA, an N+1 bit BEC is required. New modified structure with CBL has the high speed, low power and reduced area than the conventional adders.

[8] Senthilkumar.V et all-2013 Carry-select method has deemed to be a good compromise between cost and performance in any carry propagation adder design. Even though conventional carry-select adder (CSLA) is still area-consuming due to the dual ripple carry adder structure. So modified CSLA architecture has been developed using Binary to Excess-1 converter (BEC). It proposes an efficient method by modifying the gates in the BEC design. This work has a simple and efficient gate-level modification to significantly reduce the area and power of the CSLA. Depends on this modification 8-bit and 16-bit CSLA architecture have been developed. Finally it evaluates the performance of the proposed designs in terms of area and power.

[9] Saranya.K et all-2013 This work similar to the reduction of ADP by using the BEC method. It uses an efficient gate-level modification to reduce the ADP linearly. This work evaluates the performance of the proposed designs in terms of area, delay and power their products by hand with logical effort and through custom design and layout in 0.18- m CMOS process technology. Based on this modification 8-, 16-, 32-, and 64-b square-root CSLA (SQRT CSLA) architecture have been developed and compared with the regular SQRT CSLA structure. The proposed design having reduced area and power as compared with the regular SQRT CSLA with only a slight increase in the delay. The results analysis shows that the proposed CSLA structure is better than the regular SQRT CSLA.

[10] B. Ramkumar et all-2012 Design of area and power efficient high speed data path logic systems are one of the most substantial areas of research in VLSI system design. This effort uses a simple and efficient gate-level modification to significantly reduce the area and power of the CSLA. The CLSA is used in many computational systems to alleviate the problem of carry propagation delay by independently generating multiple carries and then select a carry to generate the sum according to the input bits. However, the CSLA is not area efficient because it uses multiple pairs of RCA to generate partial sum and carry by considering carry input and then the final sum and carry are selected by the mux. The basic idea of this work is to use Binary to Excess-1 converted (BEC) instead of RCA with in the regular CSLA to achieve lower area and power consumption. The main benifit of this BEC logic comes from the lesser number of logic gates than the single bit Full Adder (FA) structure. This work

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evaluates the performance of the proposed designs in terms of area, power and delay their products by hand with logical effort and through custom design and layout in 0.18-m CMOS process machinery.

Table-2. Comparison of ADP

Adder	*Area (mm)*	*Delay (ns)*	*Power (mW)*
6.CSLA	22	20.68	-
7.CSLA	111	11.15	119
8.CSLA	48	-	11
9.CSLA	0.097	0.14	0.076
10.CSLA	895	1.958	188.4

16-Bit CSLA:

[11] Syed saleem et all et all-2014 Proposed an new CSLA with D-latch structure. Though, the Regular CSLA is still area-consuming due to the dual RCA structure in the adder design. For reducing area, the CSLA will be implemented by using a single RCA and an add-one logic circuit instead of using dual RCA. The modified CSLA architecture has beed developed using BEC. This method replaces the BEC add one circuit by D-latch with enable signal. Latches are used to store an one bit information. In this RCA will act as an MSB. According to the inputs given to the adder the clock signal goes to low and high level. Experimental results are compared and the result analysis shows that the proposed architecture achieves the two folded advantages in terms of area and delay.

[12] Gagandeep Singh et all-2014 The basic idea of this work is to use Modified Binary to Excess-1 Converter (BEC) instead of RCA with Cin=1 and a simple gate level modification is done for designing a modified XOR gate which reduces the area of the circuit considerably. As RCA's and BEC make use of XOR gates in their circuits, so the total gate count of CSLA can be considerably reduced by using modified XOR gate. Analyzing the structure of Regular CSLA (R-CSLA) and Modified CSLA (M-CSLA), there is a scope to reduce the area further. Based on this modification, 16-bit Area Efficient CSLA (AE-CSLA) is designed which provides reduced area and low power which will be implemented in CADENCE VIRTUOSO using 180nm CMOS process methodology.

[13] Mugilvanan et all-2013 Carry Select Adder (CSLA) is one of the fastest adders used in many data-processing processors to perform fast arithmetic and logical functions. From the design of the CSLA, it is clear that there is a small scope for reducing the area and power intake in the CSLA. It uses a simple and efficient transistor-level modification in the BEC-1 converter to significantly reduce the area and power of the CSLA. According to this modification 16-b square-root CSLA (SQRT CSLA) architecture have been developed and compared with the SQRT CSLA architecture using ordinary BEC-1 converter. The proposed design has reduced area and power as compared with the SQRT CSLA using ordinary BEC-1 converter with only a slight increase in the delay. These works analyze the performance of the designs in terms of ADP by hand with logical effort and through Cadence Virtuoso. The analysis result shows that the new proposed CSLA structure is better than the SQRT CSLA with ordinary BEC-1 converter.

[14] Yasmeen et all-2013 A carry-select adder (CSA) can be implemented by using single ripple carry adder and an binary access code circuit instead of using dual ripple-carry adders to reduce the area and power along with speed delay. This proposes new add-one circuits using the BEC circuit and low-delay multiplexers to reduce the area and accelerate the speed of CSA, and no limitations are imposed on the design of the adder blocks. For bit length n = 16, this new carry-select adders called Square-Root CSLA (SQRT CSLA) architecture have been developed and compared with the regular SQRT CSLA architecture requires approximate 10 percent fewer gates and percent shorter delay than the original dual ripple-carry carry select adder.

[15] Veena V Nair et all-2013 Carry Select Adder (CSLA) is one of the high speed adders used in many computational systems to perform fast arithmetic operations. The modified CSLA architecture has developed using Binary to Excess-1 converter (BEC). This proposes an efficient method which replaces the BEC using D latch. The modified CSLA using BEC will reduce area and power consumption with slight increase in the delay parameter. The basic concept behind the proposed architecture is that which exchanges the BEC by D latch with enable signal. Instead of using two separate adders in the regular CSLA structure, only one adder is used to reduce the area, power intake and delay. Each of the two additions is achieved in single clock cycle. This is 16-bit adder in which the least significant bit (LSB) adder is ripple carry adder, which is 2 bit wide. The superior half of the adder i.e., the most significant bit is 14-bit wide which works according to the clock.

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New architecture will reduces the area, delay and power linearly.

Table-3. Comparison of ADP

Adder	*Area (mm)*	*Delay (ns)*	*Power (mW)*
11.CSLA	424	-	-
12.CSLA	22	-	-
13.CSLA	68	0.735	0.8733
14.CSLA	-	13	-
15.CSLA	-	17.84	324.21

32-Bit CSLA:

[16] Yogayata shrivastava et all-2014 the design of carry select adder, some few requirement of area, speed and power consumption are the main importance parameter. Carry select adder (CSLA) is one of the fast adder used to perform fast arithmetic operations as we select the carry previously and calculate the sum output for both the carry conditions i.e. for Cin=1 or Cin=0. The most fundamental arithmetic operations in any ALU's are addition. The basic idea is to implement the pipelined structure of CSLA, so that the number of stages will not activated for the whole duration of time while the only that stage is to be activated in which the computation process, at the time only pipelined stage will be retain and activated through which carry is propagating. As the carry runs from one stage to the other than the previous pipelined stage will be deactivated and next stage is activated. Thus in this manner power consumption is reduced to comparatively very low level than the carry select adders we are using today. Capable utilization of CSLA depends upon the gate level modification. In this, 32-bit linear CSLA has been modified in such a way that the pipeline architecture that we have developed consumes lowest power as well as provide a high speed.

[17] Garish Kumar Wadhwa et all-2013 proposed an area-efficient carry select adder by sharing the common Boolean logic term. After Boolean simplification, the duplicated adder cells are removed in the conventional carry select adder. Alternatively it will generate duplicate sum and carry-out signal in each single bit adder cell during pocess. By utilizing the multiplexer to select the correct output according to its previous carry-out signal, After logic simplification and sharing partial logic circuit, that needs only need one XOR gate and one inverter gate in each summation operation as well as one AND gate and one inverter gate in each and every carry-out operation. Through the multiplexer, we can able to select the correct output result according to the logic state of carry-in signal. Based on this way, the transistor count in a 32-bit carry select adder can be greatly reduced.

[18] Chyn way et all-2012 proposed an area-efficient carry select adder by sharing the common Boolean logic term. After logic simplification and sharing partial circuit, we only need one XOR gate and one inverter gate in each summation operation as well as one AND gate and one inverter gate in each carry-out operation. This duplicated carry ripple adder pair is to anticipate both possible carry input values, where one carry ripple adder is calculated as carry input value is logic "0" and another carry ripple adder is calculated as carry input value is logic "1". When the actual carry input is ready, either the result of carry "0" path or the result of carry "1" path is selected by the multiplexer according to its carry input value. Through the multiplexer, we can select the correct output result according to the logic state of carry-in signal. In this way, the transistor count in a 32-bit carry select adder can be greatly reduced from 1947 to 960. Moreover, the power consumption can be reduced from 1.26mw to 0.37mw as well as power delay product reduced from 2.14mw*ns to 1.28mw*ns.

[19] Padma devi et all-2010 Power dissipation is one of the most important design objectives in integrated circuits, after speed. Due to device portability miniaturization of device should be high and power consumption should be low. As adders are the most widely used components in such circuits, design of efficient adder is of much concern for researchers. This performance analysis of different Fast Adders. The comparison is done on the basis of three performance parameters i.e. Area, Speed and Power consumption. This present a modified carry select adder designed in different stages. Results obtained from modified carry select adders are better in area and power consumption**.**

[20 Ruiz et all-2004 This paper presents a highly area-efficient CMOS carry-select adder (CSA) with a regular and iterative-shared transistor structure very suitable for implementation in VLSI. This adder is based on both a static and compact multi-output carry look-ahead (CLA) circuit and a very simple select circuit. Comparisons with other representative 32-bit CSAs show that the proposed adder reduces the area by between 25 and 16%, the number of transistors by between 43 and 30%, and the dynamic power supply

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between 35 and 16%, while maintaining a high speed.

Table-4. Comparison of ADP

Adder	*Area (mm)*	*Delay (ns)*	*Power (mW)*
16.CSLA	-	0.589	890.37
17.CSLA	-	6.76	3.28
18.CSLA	-	3.40	3.77
19.CSLA	-	24.497	15.83
20.CSLA	-	-	-

Result and discussion

The result shows that the Carry Select Adder is more convenient adder for designing the low power applications, microprocessor design and high speed multiplications to increase the speed of the operation. In this survey it can concluded that the area, delay and power of the CSLA is reduced by using the Binary to Excess-1 Converter, Gate- level modification, Sharing the Common Boolean Logic term, D-Latch and One gate.

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